Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled)

Claims 2 - 5 (cancel)

Claims 6-10 (canceled)

Claim 11 (currently amended): A clock generator, comprising:

a high frequency clock/oscillator ~~of a wireless receiver having radio frequency circuitry and baseband circuitry~~;

a counter coupled to the clock/oscillator, wherein the counter is coupled to receive a first count value and a second count value to set an asymmetrical duty cycle; and

a controller coupled to receive an output of the counter to generate a low frequency clock with [[an]] the asymmetrical duty cycle.

Claim 12 (currently amended): The clock generator of claim 11, wherein the clock/oscillator ~~generates~~ is configured to generate an output at a high frequency relative to the low frequency clock.

Claim 13 (original): The clock generator of claim 11, wherein the counter is a down counter.

Claim 14 (original): The clock generator of claim 11, wherein the counter is a modulo counter.

Claim 15 (previously presented): The clock generator of claim 11, wherein the controller to change the position of a falling edge of a symmetrical clock relative to the position of a rising edge of the symmetrical clock to obtain the asymmetrical duty cycle.

Claim 16 (currently amended): The clock generator of claim 11, wherein the controller to minimize the nth-order harmonic and change the magnitude of ~~other~~ another harmonic ~~at a mixer of the wireless receiver~~.

Claims 17-19 (cancel)

Claim 20 (previously presented): An apparatus comprising:

an oscillator to generate a first clock signal with a first duty cycle at a first frequency;

a counter coupled to the oscillator; and

a controller to generate a second clock signal at the first frequency with a second duty cycle formed by a first transition and a second transition, the second transition initiated when a value of the counter is at a predetermined value.

Claim 21 (previously presented): The apparatus of claim 20, wherein the oscillator is at an intermediate frequency.

Claim 22 (previously presented): The apparatus of claim 20, further comprising a digital portion.

Claim 23 (previously presented): The apparatus of claim 22, wherein the oscillator and the digital portion are on a single substrate.

Claim 24 (previously presented): The apparatus of claim 23, wherein the second clock signal to be provided to the digital portion.

Claims 25 - 26 (cancel)

Claim 27 (previously presented): The apparatus of claim 20, wherein the counter is coupled to receive a first count value and a second count value to set the second duty cycle.